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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,722	10/22/2003	Sukyoon Yoon	1546.1018	3970

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EXAMINER	
HUYNH, ANDY	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,722	YOON, SUKYOON	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 October 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 October 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-15** are currently pending in the application, which claims benefit of 60/420,672 filed 10/22/2002, is acknowledged.

Drawings

The drawings are objected for the following reason.

Figures 1 and 2a-2c should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims **1-3 and 6-15** are rejected under 35 U.S.C. 102(e) as being anticipated by Kurokawa et al. (USP: 6,621,130 hereinafter referred to as "Kurokawa").

Regarding claim **1**, Kurokawa discloses in Figs. 1A-1D and the corresponding texts as set forth in column 6, line 20-column 8, line 46, a flash EEPROM unit cell comprises:

a substrate 101 on which field oxide layers 105 are formed for isolating unit cells;

a floating gate dielectric layer 108 formed between the adjacent field oxide layers, wherein the floating gate dielectric layer 108 includes a first dielectric layer 108 (laying above the writing control region 106) and a second dielectric layer 108 (laying above the writing region 107) which are connected in parallel between a source 103 and a drain 104 formed on the substrate, and the thickness of the first dielectric layer is thicker than the second dielectric layer;

a floating gate 109 formed on the floating gate dielectric layer;

a control gate dielectric layer 110 formed on the floating gate; and

a control gate 111 formed on the control gate dielectric layer.

Regarding claim **2**, Kurokawa discloses the second dielectric layer works as a tunnel oxide layer for inducing an electron-injection into the floating gate and an electron-emission from the floating gate (col. 6, line 40).

Regarding claim **3**, Kurokawa discloses in Fig. 1C the surface area of the first dielectric layer is substantially equal to that of the second dielectric layer.

Regarding claims **6-7**, Kurokawa discloses in Figs. 1A-1D and 7A, and the corresponding texts as set forth in column 6, line 20-column 8, line 46, column 15, line 64-column 16, line 10, a flash EEPROM array architecture comprises:

a plurality of bit lines B1-Bn;

a plurality of word lines W1-Wm which intersect the plurality of bit lines; and

a memory string including a plurality of unit cells 702-704 serially connected to one of the bit lines,

wherein each of the unit cells is connected to a respective word line, and the unit cell includes a first sub-cell (with a thick dielectric laying above the writing control region 106) and a

second sub-cell (with a thin dielectric laying above the writing region 107) connected in parallel between a source 103 and a drain 104, and a capacitance of a dielectric layer under a floating gate 109 of the first sub-cell is smaller than that of dielectric layer under a floating gate 109 of the second sub-cell; and

wherein the dielectric layer of the first sub-cell (laying above the writing control region 106) is thicker than that of the dielectric layer of the second sub-cell (laying above the writing region 107) (Fig. 1C).

Regarding claims **8, 9, 13 and 14**, Kurokawa discloses in Figs. 1C and 7A, a control gate 111 of the first sub-cell and a control gate 111 of the second sub-cell are connected to the same word line, and the floating gate 109 of the first sub-cell is connected to the floating gate 109 of the second sub-cell, and the floating gate of the first sub-cell and the floating gate of the second sub-cell are connected together, and the control gate of the first sub-cell and the control gate of the second sub-cell are connected together.

Regarding claims **10 and 15**, Kurokawa discloses in Fig. 1C the floating gate of the first sub-cell and the floating gate of the second sub-cell are formed between field oxide layers 105 for separating the unit cells.

Regarding claims **11 and 12**, Kurokawa discloses in Figs. 1A-1D and 7A, and the corresponding texts as set forth in column 6, line 20-column 8, line 46, column 15, line 64-column 16, line 10, a flash EEPROM array architecture comprises:

a plurality of bit lines B1-Bn;

a plurality of word lines W1-Wm which intersect the plurality of bit lines; and

a plurality of unit cells 701-704 formed at the intersection of the bit lines and the word lines;

wherein the unit cells at a row are connected to a word line W1; each of the unit cells includes a first sub-cell (with a thick dielectric laying above the writing control region 106) and a second sub-cell (with a thin dielectric laying above the writing region 107) connected in parallel between a source 103 and a drain 104 (Fig. 1C); the sources of the unit cells are connected to a common source line 712; the drains of the unit cells at a column is connected to a bit line B1 (Fig. 7A); and a capacitance of dielectric layer under a floating gate 109 of the first sub-cell is smaller than that of dielectric layer under a floating gate 109 of the second sub-cell; and

wherein the dielectric layer of the first sub-cell (laying above the writing control region 106) is thicker than that of the dielectric layer of the second sub-cell (laying above the writing region 107).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurokawa et al. (USP: 6,621,130 hereinafter referred to as "Kurokawa") in view of Lee (USP: 6,815,283).

Regarding claim **4**, Kurokawa discloses the above claimed limitations except for the thickness of the first dielectric layer is substantially equal to that of a dielectric layer of a peripheral devices formed in a flash EEPROM device to control the flash EEPROM device. Lee teaches in Figs. 1A-1G thickness of a dielectric layer 12 of a flash EEPROM device is substantially equal to that of a dielectric layer 14 of peripheral devices formed in the flash EEPROM device to control the flash EEPROM device. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form thickness of a dielectric layer of a flash EEPROM device is substantially equal to that of a dielectric layer of peripheral devices to simplify the manufacturing process.

Regarding claim **5**, Kurokawa discloses the above claimed limitations except for the floating gate is formed only on the floating gate dielectric layer. Lee teaches in Figs. 1A-1G the floating gate 13 is formed only on the floating gate dielectric layer 12. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the floating gate only on the floating gate dielectric layer, as taught by Lee in order for a self align source (SAS) annealing process.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

Andy Huynh

01/04/05

Patent Examiner